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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/808,612	03/14/2001	Thomas J. Pennello	MWI.003A	4549

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EXAMINER	
FERRIS III, FRED O	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 06/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/808,612	PENNELLO ET AL.	
	Examiner	Art Unit	
	Fred Ferris	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-35 have been presented for examination based on applicant's amendment filed on 27 January 2005. Claims 1-35 remain rejected by the examiner.

Response to Arguments

2. Applicant's arguments filed 27 January 2005 have been fully considered.

Regarding applicant's response to 112(1) rejection: The examiner withdraws the 112(1) rejection in view of applicant's amendment to the claims, specification, and arguments the claimed "hardware process" in merely a digital processor as would have been known to a skilled artisan at the time of the invention.

Regarding applicant's response to IDS and objection to the specification: The examiner withdraws the objections to the specification in view of applicant's amendment to the specification and arguments filed 27 January 2005.

Regarding applicant's response 102(e) rejections: The examiner withdraws the 102(e) rejection claim 19 in view of applicant's amendment to the claims. However, applicant's arguments relating to amended claim 1 and 23 are not persuasive. The examiner notes that the amended claim limitation that recites, "wherein said act of continuously switching comprises switching without determining whether an event of interest has occurred", can merely be interpreted as polling. (Applicants appear to concur with this interpretation based on the arguments recited on page 17, lines 1-5 of applicant's response) While applicants argue that Merks teaches a "waiting step" limited by a "time out" period while polling, the examiner finds nothing in claimed limitations of

independent claim 1 to distinguish the claimed invention over the polling process taught by Merks. The examiner has therefore interpreted claimed inventions amended "continuously switching" process to be functionally equivalent to the polling as taught by Merks.

MPEP 2106 recites the following supporting rational:

> "While it is appropriate to use the specification to determine what applicant intends a term to mean, a positive limitation from the specification cannot be read into a claim that does not impose that limitation. A broad interpretation of a claim by Office personnel will reduce the possibility that the claim, when issued, will be interpreted more broadly than is justified or intended. An applicant can always amend a claim during prosecution to better reflect the intended scope of the claim."

In this case applicant's arguments are clearly more specific than the claims require.

The examiner also notes that the claimed "extended digital processors" are simply defined by applicants specification be processors capable of performing "extended operations". (Specification page 7, line 1-5). The examiner submits that it is well established the (See: "Introduction to Computer Architecture", Stone, 1980, defining a typical example of such an extension instruction) The examiner therefore asserts that the claimed "extended operations" are inherent in the processors taught in the prior art.

The examiner therefore maintains the 102(e) rejection of claims 1 and 23.

Regarding applicant's response to 103(a) rejection: Applicant's first argue that the prior art does not teach the use of polling or periodic switching. In response, the examiner notes the applicants have not specifically claimed polling or periodic switching in the language of the claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re

Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). However, the examiner also notes that applicant's now appear to be arguing that the amended claim limitation which recites "wherein said act of continuously switching comprises switching without determining whether an event of interest has occurred" is to merely be interpreted as polling or periodic switching between processes to obtain status information. (See: applicant's response page 17, lines 1-5) The examiner submits that based on this interpretation the claimed "continuously switching" process, (i.e. polling) and subsequently "determining whether an event of interest has occurred", is anticipated by Merks using the same reasoning as noted above. This issue not withstanding, it is well established that the process of "polling" is very well known and commonly practiced in the art a means of "periodically determining the statues of a device or process" (Microsoft Computer Dictionary, 3rd Edition, 1997). Hence, a "polling" process would have necessarily been incorporated by a skilled artisan as a means of "determining whether an event of interest has occurred" between processes to obtain status information.

Regarding amended claim 19: The amended limitation to include a "simulator" process is rendered obvious by the combination of Merks and Davis as now recited below under 103(a) rejections.

Regarding response to claims 20 and 21: Claim 20 (i.e. selectively running processes while stopping others) is rendered obvious by Merks at least at column 4, lines 20-55, column 7, line 55, and in Figure 1. Claim 21 is rendered obvious by the "hold process" information disclosed by Merks at least at column 9, lines 9-43.

Regarding applicants response to Official Notice rejection of claims 8-10: The examiner maintains that it is well established in the art that an "extension instruction" merely refers to processor's extended instruction capability such as, "a program module that adds functionality to or extends the effectiveness of a program", (See: "extension" definition (3), Microsoft Computer Dictionary, 3rd Edition, 1997) i.e. an "extension" of a standard instruction's capability such as reserved processor instruction supplied by a processor manufacturer. The examiner also submits herewith pages 182 and 183 the textbook "Introduction to Computer Architecture", Stone, 1980, defining a typical example of such an extension instruction. The examiner therefore maintains the Official Notice that the claimed "extension instruction" was known to a skilled artisan at the time of the invention.

Regarding 103(a) rejections motivation to combine: The examiner contends that the motivation to combine Merks and Davis is proper and in accordance with MPEP guidelines for the following reasons. MPEP 2143.01 Suggestion or Motivation To Modify the References first recites:

"There are three possible sources for a motivation to combine references: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art." In re Rouffet, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998)

Therefore, in suggesting a motivation to combine, the examiner specifically focused his motivation on the knowledge of persons of ordinary skill in the art. More specifically, that a skilled artisan would have made an effort to become aware of what capabilities had been developed in the market place, and hence would have knowingly

modified Merks with the teachings of Davis. (See: 103(a) rejection below) MPEP 2144 Sources of Rationale Supporting a Rejection Under 35 U.S.C. 103 recites:

> "The rationale to modify or combine the prior art does not have to be expressly stated in the prior art; the rationale may be expressly or impliedly contained in the prior art or it may be reasoned from knowledge generally available to one of ordinary skill in the art, established scientific principles, or legal precedent established by prior case law. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). See also In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000) (setting forth test for implicit teachings); In re Eli Lilly & Co., 902 F.2d 943, 14 USPQ2d 1741 (Fed. Cir. 1990) (discussion of reliance on legal precedent); In re Nilssen, 851 F.2d 1401, 1403, 7 USPQ2d 1500, 1502 (Fed. Cir. 1988) (references do not have to explicitly suggest combining teachings)"

The examiner has simply asserted that a skilled artisan tasked with solving the problem of debugging processes in a distributed (multi) processor environment (i.e. as taught by Merks), and object subclasses for hardware and simulation processes (i.e. as taught by Davis), and further having access to the teachings of Merks and Davis, would have looked to the prior art and hence would have knowingly modified the teachings of Merks, with the teachings of Davis in order to gain the advantage of reduced cost and development time. Specifically, a skilled artisan working in this obviously competitive environment would have made an effort to become aware of what capabilities had already been developed in the market place, and hence would have been aware of, and known to seek out the relative teachings of the problem to be solved. Namely, the teachings of Merks and Davis.

MPEP 2143.01 Suggestion or Motivation To Modify the References further recites the following supporting rational:

> Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. **"The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those**

of ordinary skill in the art." In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000).

The examiner therefore appears to have established an implicit showing that in view of the combined teachings of the prior art, the relative knowledge of one skilled in the art, and in particular, the nature of the problem to be solved, there exists an obvious motivation to combine the references as noted in the 103(a) rejection below.

For the reasons set forth above the examiner maintains the 102(b) and 103(a) rejections.

Claim Interpretation

*3. Applicants are disclosing and claiming a method and apparatus for debugging distributed programs by identifying and initializing processes, executing a thread to control processes, and cycling between processes to monitor status. As currently written, the independent claims appear to be broadly drawn to subject matter that is commonly known in the art as **debugging of concurrent processes**. (See: "Debugging of Concurrent Processes", S. Grabner et al, IEEE 1066-6192/95, IEEE 1995, for example) Accordingly, the examiner has interpreted the claimed limitations relating to debugging of distributed programs as equivalent to techniques used in debugging of concurrent processes and has applied art rejections accordingly. (See: 102/103 rejections below)*

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,516,460 issued to Merks et al.

Independent claims 1 and 23 are drawn to:
Method for debugging distributed programs by:
Identifying processes
Initializing processes
Executing single thread of control among processes
Continuously switching between processes (i.e. polling) to obtain related status

Regarding independent claims 1 and 23: Merks discloses debugging distributed programs over multiple processors, initializing processors, executing a control thread, switching between processes and obtaining status information. (Abstract, Background, CL1-L55 - CL4-L55, Fig. 1) For example, at column 9, line 5 Merks recites:

"the preferred embodiment of the present invention allows for simultaneous **debugging of multiple related processes** in a Windows NT and Windows 95 environment by having the call to WaitForDebugEvent( ) specify a **timeout period** and for **the loop to continuously poll for events from all debuggee processes**. The pseudocode is as follows:
// executing on **"special" debugger thread**
// DEBUG_EVENT debug_event;
for (;;)
// let all the debuggee processes run that are supposed to run"

Merks teaches the elements of the claimed limitations of the present invention as follows:

- Method for debugging distributed programs: Merks discloses debugging processes in a distributed (multi) processor environment (Abstract, Background, CL4-L66, CL5-L5, 10, 15-35, CL11-L26). (Merks also discloses the storage medium for data CL11-L11)

- Identifying processes: Merks discloses (selectively) identifying among parent/child processes (CL5-L27-35, CL7-L39, CL10-L27-29, Fig. 4) during the debugging process.

- Initializing processes: Merks discloses initiating processes with initial parameters such as process information, code, variables, and indicators, (i.e. initializing the processes) and starting/restarting the debugging of processes (CL8-L44-51, CL11-L28).

- Executing single thread of control among processes: Merks discloses executing a thread (single) as part of the control process among processes (CL2-L7-11, CL9-L54-58).

- Continuously switching between processes to obtain related status: Merks teaches continuously polling between processes in order to monitor the "status" of each pending debug process (CL9-L5-58).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,516,460 issued to Merks et al in view of U.S. Patent 6,230,307 issued to Davis et al.

Independent claims 1, 19 and 23 are drawn to:
Method for debugging distributed programs by:
Identifying processes
Initializing processes
Executing single thread of control among processes
Continuously switching between processes (i.e. polling) to obtain related status

Regarding independent claims 1, 19, and 23: Merks discloses debugging distributed programs over multiple processors, initializing processors, executing a control thread, switching between processes and obtaining status information. (Abstract, Background, CL1-L55 - CL4-L55, Fig. 1) For example, at column 9, line 5 Merks recites:

"the preferred embodiment of the present invention allows for simultaneous **debugging of multiple related processes** in a Windows NT and Windows 95 environment by having the call to WaitForDebugEvent( ) specify a **timeout period** and for **the loop to continuously poll for events from all debuggee processes**. The pseudocode is as follows:
// executing on **"special" debugger thread**
// DEBUG_EVENT debug_event;
for (;;)
// let all the debuggee processes run that are supposed to run"

Merks renders obvious the elements of the limitations of independent claims 1, 19, and 23 as follows:

- Method for debugging distributed programs: Merks discloses debugging processes in a distributed (multi) processor environment (Abstract, Background, CL4-L66, CL5-L5, 10, 15-35, CL11-L26).

- Identifying processes: Merks discloses (selectively) identifying among parent/child processes (CL5-L27-35, CL7-L39, CL10-L27-29, Fig. 4) during the debugging process.

- Initializing processes: Merks discloses initiating processes with initial parameters such as process information, code, variables, and indicators, (i.e. initializing the processes) and starting/restarting the debugging of processes (CL8-L44-51, CL11-L28).

- Executing single thread of control among processes: Merks discloses executing a thread (single) as part of the control process among processes (CL2-L7-11, CL9-L54-58).

- Continuously switching between processes to obtain related status: Merks teaches continuously polling between processes in order to monitor the "status" of each pending debug process (CL9-L5-58). Merks polls to monitor the status of process information, code, variables, and indicators (CL8-L44-51, CL11-L28) in the debugging process.

However, Merks does not explicitly disclose the limitations of dependent claims 2-4 relating to:

- *simulation process*
- *hardware process*
- *analyzing status for errors*
- *defining object classes*
- *defining object subclasses for hardware and simulation processes*

Regarding dependent claims 2-4: Davis teaches the elements of the limitations of independent claims 2-4 as follows:

- *simulation process: Davis discloses the simulation (emulation) for both a* ***hardware and software*** *realization of circuit (object) elements (Abstract, CL1-L25-55, CL4-L 51-58, CL24-L16-18, Figs. 1, 6 and 9).*
- *hardware process: As noted above, Davis discloses the simulation (emulation) for both a* ***hardware and software*** *realization of circuit (object) elements (Abstract, CL1-L25-55, CL4-L 51-58, CL24-L16-18, Figs. 1, 6 and 9).*
- *analyzing status for errors: Davis discloses determining the status (i.e. analyzing status) of various object elements and detecting and responding to the occurrence of errors. (CL12-L23-33, Fig. 17, CL42-L49) (Merks discloses monitoring status as noted above)*
- *defining object classes: Davis discloses defining hardware object classes for emulated (simulated) circuit element (CL9-L54-67, CL10-L1-39, Figs. 11, 12)*
- *defining object* ***subclasses*** *for hardware and simulation processes: Davis further discloses defining subclasses for the hardware simulation (emulation) processes (CL11-L43-56, CL9-L5-24, Fig. 15)*

Merks further does not explicitly disclose the additional limitations of dependent claims 5-13 relating to:

- *first instance variable controlling processes*
- *dynamically changing polling time of process based on status*
- *interface for defining/accessing library of hardware processes*

- *library includes extension instructions*
- *initializing hardware simulator processes*
- *dynamically loadable library*

Regarding dependent claims 5-13: Davis teaches the elements of the limitations of independent claims 5-13 as follows:

- *first instance variable controlling processes: Davis discloses using variables in the thread based scheduling and controlling of processes from an initial (first) state (CL3-L32-37, CL7-L56,CL9-L25-53, CL12-L15-23, Fig. 17).*
- *dynamically changing polling time of process based on status: Davis discloses the use of various primitives for setting parameters relating to dynamically scheduling/dispatching tasks which can effect (change) the scheduling (polling) time for process execution and management (CL12-L15-37). (Merks also discloses a variable rate polling time as noted above)*
- *interface for defining/accessing library of hardware processes: Davis discloses defining, accessing, and interfacing to a library of dynamically re-configurable hardware processes. (CL5-L52-64, CL6-L14-33, CL8-L39-64, Figs. 3, 4, 9)*
- *library includes extension instructions: Extension instructions are reserved processor instruction set by the processor manufacturer, and hence would have been an obvious feature to include in the library of hardware processes. (See applicant's specification page 7, line 5-12)*
- *initializing hardware simulator processes: Davis discloses beginning the thread controlled hardware simulation (emulation) process from a known initial (i.e. initialized) state. (CL9-L20-25, Fig 10)*

- *dynamically loadable library: Davis discloses a dynamically loadable and re-usable library (CL8-L54 to CL9-L5).*

Regarding independent claims 14, 20-22, and 24: In addition to the limitations previously addressed above, independent claims 14, 20-22, and 24 include additional limitations relating to "one hardware process", "heterogenous processors", and a distributed "multi-processing" environment. As noted above, Davis discloses the simulation (emulation) for ***hardware process*** *realization of circuit (object) elements (Abstract, CL1-L25-55, CL4-L 51-58, CL24-L16-18, Figs. 1, 6 and 9). Both Davis and Merks support heterogenous processors since the library of Davis includes hardware processes from various integrated circuit manufactures and Merks method of debugging concurrent processes is capable of operating on hardware from various manufacturers as also noted above. Both Davis and Merks disclose simulation (emulation) debugging in a distributed multi-processor environment. (See Davis: Fig. 8, and Merks: Abstract) Davis further discloses an apparatus (claim 24) capable of carrying out the processes of the claimed limitations (Fig. 4).*

It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teachings of Merks relating to debugging distributed programs over multiple processors, with the teachings of Davis relating to simulation (emulation) of ***hardware processes*** *of library based circuit (object) elements, to realize the claimed invention. An obvious motivation exists since this area of technology is highly competitive with many techniques for debugging concurrent*

processes available in the market place (see Grabner Abstract/Conclusion, for example) Accordingly, a skilled artisan would have made an effort to become aware of what capabilities had already been developed in the market place and, hence, would have been motivated to modify the teachings of Merks with the teachings of Davis in order to reduce development time and cost.

Regarding new claims 25, 27, 28, and 30: These claims include limitations relating to the determination of status information by periodically switching (i.e. polling) to determine status. These claims are therefore rendered obvious using the same reasoning as recited above. Namely, that the process of "polling" is very well known and commonly practiced in the art a means of "periodically determining the statues of a device or process" (Microsoft Computer Dictionary, 3rd Edition, 1997). Hence, a "polling" process would have necessarily been incorporated by a skilled artisan as a means of "determining whether an event of interest has occurred" between processes to obtain status information and if a debug event has occurred. Therefore, such features would have knowingly been incorporated by a skilled artisan using the same reasoning as set forth above.

Regarding new claims 26, 29: These claims merely include additional limitations relating to extended processors. The examiner has asserted that the claimed "extended digital processors" are simply defined by applicants specification be processors capable of performing "extended operations". (Specification page 7, line 1-5). The examiner has submitted that it is well established that processors included extended instruction operations. (See: "Introduction to Computer Architecture", Stone, 1980, defining a

typical example of such an extension instruction) The examiner therefore submits that the claimed "extended operations" would have knowingly been incorporated by a skilled artisan using the same reasoning as set forth above.

6. Claims 31-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,516,460 issued to Merks et al in view of U.S. Patent 6,230,307 issued to Davis et al in further view of U.S. Patent 5,101,491 issued to Katzeff.

Regarding claims 31-35: The combination of Merks and Davis renders obvious the limitations relating to debugging distributed programs over multiple processors and simulation of hardware processes of library based circuit elements and previously cited above.

Merks further does not explicitly disclose the elements relating to language independent debugging.

Katzeff teaches a language independent method (CL1-L55 to CL2-L11, Summary of Invention) of debugging process entities inclusive of a simulation of a hardware process (Figs. 1-3, 8, 9).

It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to further modify the teachings of Merks and Davis relating to debugging distributed programs over multiple processors, and simulation (emulation) of ***hardware processes*** *of library based circuit (object) elements, with the teachings of Katzeff relating to language independent debugging, to realize the claimed invention. An obvious motivation exists since this area of technology is highly competitive with*

many techniques for debugging concurrent processes available in the market place (see Grabner Abstract/Conclusion, for example) Accordingly, a skilled artisan would have made an effort to become aware of what capabilities had already been developed in the market place and, hence, would have been motivated to further modify the teachings of Merks and Davis with the teachings of Katzeff in order to realize the claimed invention and gain the advantage of reduced development time and cost.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, ***THIS ACTION IS MADE FINAL****. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).*

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, careful consideration should be given prior to applicant's response to this Office Action.

U.S. Patent 6,718,294 issued to Bortfeld teaches debugging concurrent processes in a multi-simulator environment.

"Debugging of Concurrent Processes", S. Grabner et al, IEEE 1066-6192/95, IEEE 1995, teaches debugging concurrent processes in a multi-simulator environment.

"A Concurrent Program Debugging Environment using Real-time Replay", E.H. Piak et al, IEEE 0-8186-8227-2/97, IEEE 1997, teaches debugging concurrent processes in a multi-simulator environment.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 571-272-3778 and whose normal working hours are 8:30am to 5:00pm Monday to Friday. Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 571-272-3700. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached at 571-272-3780. The Official Fax Number is: (703) 872-9306

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May 25, 2005

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PRIMARY EXAMINER